Amendments to the Specification:

Please amend the specification as follows:

On page 8, please insert the following paragraph between the third and fourth paragraphs (between lines 11 and 12):

Figure 1F-3 is a simplified, partial, exploded, cross-sectional view of a post-etched multi-layer semiconductor structure of Figure 1D having low-K dielectric layers, as covered with a passivation-capping layer, in accordance with still another embodiment of the present invention.

On Page 19, please replace the First Paragraph, lines 1-7 with the following paragraph:

Following the introduction of the low-K dielectric material 111, as illustrated in Figure 1F-2, the post-etched low-K dielectric semiconductor structure 100" is covered with a passivation-capping layer 118', in accordance with one implementation of the present invention. As shown, the passivation-capping layer 118' functions as a sealing passivation layer as well as a lid. As depicted, the passivation-capping layer 118', the first through seventh dielectric layers 110a'-110g', and the substrate 102 form a semiconductor structure 100" that has high structural integrity with low capacitive delay. Figure 1F-3 illustrates the post-etched multi-layer semiconductor structure 100' of Figure 1D having low-K dielectric layers, as covered by the passivation-capping layer 118', in accordance with another embodiment of the present invention.